A New Cost Effective Technique For Accelerated PCB Testing

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Reliability testing has become increasingly important to the electronics and PCB industries for a variety of reasons. There has been a significant introduction of new and updated Copper clad laminate materials; a variety of new interconnection techniques (i.e. blind, buried, stacked, bump, post, filled, etc.) and of innovations in lamination, hole preparation, drilling and plating techniques. All have increased the difficulty of measuring influence on interconnection reliability, requiring to find new evaluation methods while reducing energy consumption and cycle times.

Figure 1 - HATS thermal chamber with 36 coupons

Reliability testing of PCB interconnects has historically been performed using dual chamber thermal shock techniques that date back to the 1950's. This well proven methodology for thermal shock testing is unfortunately both lengthy and costly. With cycle times typically at 60 minutes, a 1000 cycle test would take an intolerable 42 days to complete. Proper electrical monitoring of the samples during dual chamber testing has also been difficult and is many times not implemented properly. While there have been attempts to accelerate this type of cycling reliability test, no technique to date has been able to correlate to the results obtained by dual chamber thermal shock systems. A new methodology has been developed that significantly reduces the time required to perform interconnection reliability testing, increases the accuracy of electrical monitoring and correlates to dual chamber techniques.

New motivations

In the electronics and printed circuit board industries, reliability testing has become increasingly important in recent years. Here are some motivations:

- new and improved Copper clad laminate materials (halogen-free, conductive anodic filament (CAF) resistant, suitable for high-frequencies applications, etc.) have been introduced into the printed circuit board industry;
- many innovative interconnection designs and techniques have been developed in electronics assemblies and packages, as well as in PCB projects, such as blind and buried holes, microvias, stacked vias, bumps, etc.);
- new processing techniques (Lead-free, drilling, hole and surface cleaning and preparation, plating, deposition changes, filling, lamination, etc.) are now on stage.

All have increased the difficulty of evaluating and measuring the influence on interconnection reliability. If these manufacturing issues are coupled with the need to make improvements in the technology required

Table 1 – Highly Accelerated Thermal Shock vs. Current Induced Heating methods

HATS	IST
Range: -60 to 160°C	Range: 27°C minimum
Heating method: air 36 Coupons	Heating method: DC current 6 Coupons
4 nets each 144 nets total	2 nets each 12 nets total
Coupon emulates PCB design Typical cycle time: 3.5 min. from 25 to 150°C 6 min. from -45 to 150°C	Coupons with special heating nets Typical cycle time: 3 min. from 25 to 150°C

for next-generation designs, you have a wealth of reasons to warrant a rapid cost effective method to measure interconnection reliability.

Highly accelerated thermal shock

Highly Accelerated Thermal Shock (HATS) is a new technology based on traditional air-to-air methods to evaluate the reliability of electronic interconnections within the circuit board and connections between the packages and the circuit board. The technique utilises a single chamber that is alternately heated and cooled by an air stream that is forced past the samples. The unit is capable of temperatures from -60°C to +160°C. Thirty-six coupons (Figure 1), each with four daisy-chain nets, can be tested in one chamber load. Precision electrical resistances of each of the 144 nets are monitored during thermal cycling, providing data that shows the degradation of the nets during the test.

Test coupons are designed with software that is run from the Internet with a web browser. Coupon sizes range from a minimum of 12.7mm by 25.4mm to a maximum size of 50.8mm by 25.4mm. Designs can be created for circuits with two to eighty layers. Specific design parameters for each of the four daisy-chain nets include via type (through, blind, buried, or stacked), hole size, land size, interconnect track width, interconnect sequence, and grid size. Further, each net can include/exclude teardrops, non-functional lands, and soldermask coverage. Upon completion of the design process, the Gerber files are "zipped" and e-mailed to the designer. The design can be added to available panel area and manufactured with the product, or placed on test panels to evaluate the reliability of alternative processes.

The coupons, on which connectors have been soldered, are inserted into the thermal chamber after preconditioning that simulates solder and rework cycles. The system is programmed and controlled by a personal computer running the Windows operating system. A typical cycle time for a fully loaded chamber of 1.6mm-thick coupons from -40°C to +145°C is six minutes. The HATS system provides data files that report the high and low resistance values for each net during each cycle. These data are read and processed by analysis software that creates tables and graphs of the results.

Comparing reliability testing techniques

Current PTH reliability techniques include a) thermal stresses (solder pot; reflow oven); and b) thermal shock (air-to-air dual chambers; liquid-to-liquid; current induced heating (IST); c) Highly Accelerated Thermal Shock).

The HATS system emulates traditional air-to-air techniques to impart thermal stresses upon the test samples. However, unique design features provide improved performance compared to traditional dual chamber methods. By alternately providing hot and cold air streams that flow across stationary samples, the electrical resistance of each daisy-chain net is easily monitored during the entire test, eliminating the need for long cables that must be moved from a hot chamber to a cold chamber and back again. Heat transfer to/from the samples is improved due to high volume forced convection air flow. Some comparisons between HATS and IST are shown in Table 1.

With HATS, the thermal mass of the chamber is minimised, providing for efficient heating and cooling of the samples. The result of these improvements is a shorter cycle time, in most cases cutting the time by more than a factor of 7, shrinking a 1000 cycle test from 42 days to 5-7 days.